WHAT IS CLAIMED IS:

1. A content addressable memory for making a comparison between input information and retrieval information, comprising:

a memory array including a plurality of memory cell rows storing said retrieval information, and a redundant memory cell row repairing a faulty memory cell row;

a first shift circuit shifting; if necessary, each of at least one memory cell row to be accessed in a first direction during data reading and data writing;

a second shift circuit shifting each of said at least one memory cell row shifted in said first direction by said first shift circuit in a second direction opposite to said first direction in data retrieving;

an address producing circuit producing an intended address based on information transmitted from each of said memory cell rows through said second shift circuit in said data retrieving;

a plurality of stages of latch circuits provided corresponding to respective addresses of said plurality of memory cell rows, and each latching a shift signal instructing an operation of shifting the corresponding memory cell row in said first and second shift circuits; and

a shift signal producing portion producing said shift signal to be latched by each of said latch circuits based on a faulty address of said faulty memory cell row.

2. The content addressable memory according to claim 1, wherein said shift signal producing portion includes:

a storing portion storing said faulty address of said faulty memory cell row, and

a control circuit issuing said shift signal to each of said latch circuits corresponding to the address of memory cell row in sequence among said plurality of stages of latch circuits, on the address of said faulty memory cell row stored in said storing portion.

3. The content addressable memory according to claim 2, wherein said control circuit includes:

an address counter counting said addresses corresponding to said plurality of memory cell rows one by one in ascending order,

a comparing circuit making comparison between the address provided from said address counter and said faulty address of said faulty memory cell row stored in said storing portion,

a signal latch portion setting said shift signal in a binary form based on a result of said comparison, and latching said shift signal for outputting to each of said latch circuits, and wherein,

each of said latch circuits includes an input control portion sequentially receiving said shift signal issued from said signal latch portion in synchronization with counting by said address counter.

4. The content addressable memory according to claim 1, wherein said memory array further includes a plurality of match lines provided corresponding to the plurality of memory cell rows, respectively, and each determining whether said input information matches with a portion of said retrieval information stored in the corresponding memory cell row;

said content addressable memory further comprises:

a plurality of precharge units provided corresponding to said plurality of match lines for precharging the corresponding match lines to a predetermined voltage level, respectively, and

a plurality of precharge control portions activating said plurality of precharge units before said data retrieval, respectively;

first and second logical data instructing and not instructing said shift operation are set based on said shift signal in each of said latch circuits; and

each of said precharge control portions activates the corresponding precharge unit when said second logical data is set in the latch circuit corresponding to the same memory cell row, and activates the corresponding precharge unit when said first logical data is set in the latch

circuit in previous stage of said corresponding latch circuits when said first logical data is set.

5. The content addressable memory according to claim 1, wherein said memory array further includes match lines provided corresponding to said memory cell rows including said redundant memory cell row, respectively, and determining whether said input information matches with a portion of said retrieval information stored in each of said memory cell rows;

each of said memory cell rows including said redundant memory cell row has a plurality of memory cells each storing one bit of data; and

each of said memory cells has:

a first cell unit having a first storage node holding first data,

a second cell unit having a second storage node holding second data, and

a comparing circuit comparing a pair of data held on said first and second storage nodes with input data forming said input information, and selectively driving the match line corresponding to a result of the comparison.

6. The content addressable memory according to claim 1, wherein said first and second shift circuits and said plurality of stages of latch circuits neighbor to one side of said memory array.

7. The content addressable memory according to claim 1, wherein said first shift circuit includes a plurality of row select units corresponding to said plurality of memory cell rows during said data reading and writing, respectively, each performing the shifting in said first direction based on said shift signal, and executing the access to the corresponding memory cell rows based on received addresses of said plurality of memory cell rows, respectively.

8. A content addressable memory for making a comparison between

input information and retrieval information, comprising:

a memory array including a plurality of memory cell rows storing said retrieval information, and a plurality of redundant memory cell rows repairing a faulty memory cell row,

said plurality of memory cell rows being divided into a plurality of memory cell row groups, each group including a predetermined number of the memory cell rows, corresponding to a part of bits of addresses of said plurality of memory cell rows;

a first shift circuit shifting, if necessary, each of at least one memory cell row group to be accessed in a first direction during data reading and data writing;

a second shift circuit shifting each of said at least one memory cell row group shifted in said first direction by said first shift circuit in a second direction opposite to said first direction in data retrieving;

an address producing circuit producing an intended address based on information transmitted from each of said memory cell row group through said second shift circuit in said data retrieving;

a plurality of stages of latch circuits provided corresponding to respective addresses of said plurality of memory cell row groups, and each latching a shift signal instructing an operation of shifting the corresponding memory cell row group in said first and second shift circuits; and

a shift signal producing portion producing said shift signal to be latched by each of said latch circuits based on a faulty address of said faulty memory cell row.

9. The content addressable memory according to claim 8, wherein

said first shift circuit includes a plurality of row select units corresponding to said plurality of memory cell row groups during said data reading and writing, respectively, each performing the shifting in said first direction based on said shift signal, and executing the access to the corresponding memory cell rows based on received addresses of said plurality of memory cell rows, respectively, and

the one row select unit corresponding to said part of bits of addresses of said plurality of memory cell rows is selected from said plurality of row select units, and one memory cell row included in the memory cell row group corresponding to said selected row select unit is accessed based on the remaining bits of addresses.

10. A content addressable memory for making a comparison between input information and retrieval information, comprising:

a memory array including a plurality of memory cell rows storing said retrieval information, and a redundant memory cell row repairing a faulty memory cell row;

a first shift circuit shifting, if necessary, each of at least one memory cell row to be accessed in a first direction during data reading and data writing;

a second shift circuit shifting each of said at least one of memory cell row shifted in said first direction by said first shift circuit in a second direction opposite to said first direction in data retrieving;

an address producing circuit producing an intended address based on information transmitted from each of said memory cell rows through said second shift circuit in said data retrieving; and

a control circuit controlling said first and second shift circuits based on a faulty address of said faulty memory cell row, wherein

said memory array further includes match lines provided corresponding to said memory cell rows including the redundant memory cell row, respectively, and determining whether said input information matches with a portion of said retrieval information stored in said respective memory cell rows,

each of said memory cell rows including said redundant memory cell row has a plurality of memory cells each storing one bit of storage data, and

each of said memory cells includes:

a first cell unit having a first storage node holding first data,

a second cell unit having a second storage node holding second data, and

a comparing circuit comparing a pair of data held on said first and second storage nodes with input data forming said applied input information, and selectively driving the corresponding match line in accordance with a result of the comparison.